REMARKS

Claims 1-16 are pending in the present application. New claims 17-20 are added above. Claims 1, 9, and 14 are amended above. Claims 5-8 are withdrawn from consideration as being drawn to a non-elected species. Entry of the claim amendments and new claims are respectfully requested.

Applicants note with appreciation that claims 13-16 are allowed and that claims 2 and 10 contain allowable subject matter, as stated in the Office Action at page 4, first paragraph. New claim 17 is claim 2 rewritten in independent form. New claim 19 is claim 10 rewritten in independent form. Entry and allowance of new claims 17 and 19, and dependent claims 18 and 20, are respectfully requested.

In addition, allowable dependent claim 14 is amended to correct clerical errors, in particular, to introduce proper antecedents into claim 14. Entry and allowance of amended claim 14 are respectfully requested.

Claims 1, 3, 4, 9, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of Choi (United States Patent No. 6,272,053). Reconsideration and removal of the rejections, and allowance of the claims, are respectfully requested.

The present invention as claimed in amended independent claim 1 is directed to a semiconductor memory integrated circuit, comprising a "plurality of first data IO pads," a "plurality of address and instruction pads," and a "plurality of second data IO/address pads," which are "arranged in groups adjacent each other." The "plurality of first data IO pads" are "adjacent to a first side of the plurality of address and instruction pads." The "plurality of second data IO/address pads" are "adjacent to a second side of the plurality of address and instruction

pads opposite the first side." "Each of the plurality of the second data IO/address pads" is used as a "second data IO pad" in response to a "control signal" when "packaged into a first package form" and is used as an "address pad" in response to the "control signal" when "packaged into a second package form."

The present invention as claimed in amended independent claim 9 is directed to a semiconductor memory integrated circuit, comprising a "plurality of data IO pads," a "plurality of address and instruction pads," and a "plurality of generic pads," which are "arranged in groups adjacent each other." The "plurality of data IO pads" are "adjacent to a first side of the plurality of address and instruction pads." The "plurality of generic pads" are "adjacent to a second side of the plurality of address and instruction pads opposite the first side." "Each of the plurality of generic pads" is used as a "data IO pad" in response to a "control signal" when "packaged into a first package form" and is used as an "address pad" in response to the "control signal" when "packaged into a second package form."

It is submitted that the combination of AAPA and Choi fails to teach or suggest a "plurality of first data IO pads," a "plurality of address and instruction pads," and a plurality of "second data IO/address pads," which are "arranged in groups adjacent each other," wherein the "plurality of first data IO pads are adjacent to a first side of the plurality of address and instruction pads" and the "plurality of second data IO/address pads are adjacent to a second side of the plurality of the address and instruction pads opposite the first side," as claimed in amended independent claim 1. It is further submitted that the combination of AAPA and Choi fails to teach or suggest a "plurality of data IO pads," a "plurality of address and instruction pads," and a "plurality of generic pads," which are "arranged in groups adjacent each other," wherein the "plurality of data IO pads are adjacent to a first side of the plurality of address and instruction pads" and the "plurality of generic pads are adjacent to a second side of the plurality of address and instruction pads opposite the first side," as claimed in amended independent claim 9.

With regard to AAPA, the Office Action at page 2 states that "Fig. 2 of this application already shows a semiconductor memory circuit in package form (IC 20), which includes at least a plurality of first data IO pads (1DQ), address and instruction pads (ADD, CMD), and second data IO pads, which are all arranged in different groups adjacent to each other." Applicant respectfully disagrees with this statement. In particular, Applicant submits that the second data IO balls 2DQ of AAPA are neither "second data IO/address pads," as claimed in claim 1 nor "generic pads," as claimed in claim 9, but rather the IO balls 2DQ of AAPA represent ball contacts that are bonded to the bonding pads 12-1, 12-2 via bonding wires. In the packaging configuration of FIG. 2, the "pads" 12-1, 12-2 (indicated by small squares) are located on the semiconductor memory IC 12, while the "balls" 1DQ, ADD/CMD, 2DQ (indicated by small circles) are arranged at the perimeter of the package 20.

Along these lines, as illustrated at least at FIG. 2 of the present specification, data IO pads 12-1 are disclosed in AAPA as being adjacent to address and instruction pads 12-2 in the semiconductor memory IC 12. AAPA further discloses that first data IO balls 1DQ are arranged on a left side of address and instruction balls ADD, CMD, and that second data IO balls 2DQ are arranged on a right side of address and instruction balls ADD, CMD at the perimeter of the BGA packaged semiconductor device 20, which, in the conventional BGA configuration of FIG. 2, is problematic because the distance between the data IO pads 12-1 and the second IO balls 2DQ is too far (see FIG. 2 and page 2, paragraphs [0009] - [0011] of the present specification). There is no teaching or suggestion in AAPA of a "plurality of second data IO/address pads," as claimed in amended independent claim 1, or of a "plurality of generic pads," as claimed in amended independent claim 9. Instead, AAPA discloses a conventional pad configuration of the semiconductor memory IC, whereby the data IO pads 12-1 of the IC 12 are only to one side, i.e., the left side, of the address and instruction pads 12-2. There is no teaching or suggest in AAPA of providing "data IO/address pads"or "generic pads" on the right side of the address and instruction pads 12-2. It therefore follows that the AAPA does not teach or suggest a "plurality of second data IO/address pads" that are "adjacent to a second side of the plurality of address and

instruction pads opposite the first side," as claimed in amended independent claim 1, or a "plurality of generic pads" that are "adjacent to a second side of the plurality of address and instruction pads opposite the first side," as claimed in amended independent claim 9.

With regard to Choi, there is likewise no mention in Choi of a "plurality of second data IO/address pads" that are "adjacent to a second side of the plurality of address and instruction pads opposite the first side," as claimed in amended independent claim 1, or a "plurality of generic pads" that are "adjacent to a second side of the plurality of address and instruction pads opposite the first side," as claimed in amended independent claim 9. Instead, Choi discloses a semiconductor memory device comprising data and address signals that are transmitted between an external circuit and an internal memory through a multi-pad M-PAD (see Choi, FIG. 3A and page 3, lines 28-31). However, there is no teaching or suggestion of the multi-pad M-PAD of Choi being a "plurality of second data IO/address pads" that are "adjacent to a second side of" a "plurality of address and instruction pads," as claimed in amended independent claim 1, or a "plurality of generic pads" that are "adjacent to a second side of" a "plurality of address and instruction pads," as claimed in amended independent claim 9.

In addition, it is submitted that the combination of AAPA and Choi fails to teach or suggest "each of the plurality of the second data IO/address pads" that is "used as a second data IO pad in response to a control signal when packaged into a first package form" and that is "used as an address pad in response to the control signal when packaged into a second package form," as claimed in amended independent claim 1. It is further submitted that the combination of AAPA and Choi fails to teach or suggest "each of the plurality of generic pads" that is "used as a data IO pad in response to a control signal when packaged into a first package form" and that is "used as an address pad in response to the control signal when packaged into a second package form," as claimed in amended independent claim 9. For reasons described above, AAPA fails to teach or suggest "second data IO/address pads," as claimed in claim 1 or "generic pads," as claimed in claim 9. With regard to Choi, Choi discloses an address enable signal /AE that is

generated from a memory controller (see Choi, FIG. 3A and column 3, lines 31-34). When the address enable signal /AE is at a low level, address signals are input into a multi-pad (see Choi, column 3, lines 36-38). When the address enable signal /AE is at a high level, data signals are input into a multi-pad (see Choi, column 3, lines 38-41). However, there is no mention in Choi of the multi-pads being "second data IO/address pads," each being used as a "second data IO pad in response to a control signal when packaged into a first package form" and each being used as an "address pad in response to the control signal when packaged into a second package form," as claimed in claim 1, nor is there any mention in Choi of the multi-pads being used as "generic pads," each being used as a "data IO pad in response to a control signal when packaged into a first package form" and being used as an "address pad in response to the control signal when packaged into a second package form," as claimed in claim 9. Thus, in contrast to the present invention, there is no relationship in Choi between a "control signal" and a "first package form" or a "second package form." In other words, in Choi, a multi-pad receives either address or data signals in response to the address enable signal /AE, regardless of package form. Thus, for at least these reasons, it follows that multi-pads of Choi are neither "second data IO/address pads," as claimed in amended independent claim 1 nor "generic pads," as claimed in amended independent claim 9.

It is therefore submitted that neither AAPA nor Choi teaches or suggests certain specified elements of the invention. Specifically, neither reference, taken alone or in combination, teaches or suggests "plurality of second data IO/address pads" that are "adjacent to a second side of the plurality of address and instruction pads opposite the first side," as claimed in amended independent claim 1, or a "plurality of generic pads" that are "adjacent to a second side of the plurality of address and instruction pads opposite the first side," as claimed in amended independent claim 9. In addition, neither reference, taken alone or in combination, teaches or suggest "each of the plurality of the second data IO/address pads" that are used as a "second data IO pad in response to a control signal when packaged into a first package form" and that are used as an "address pad in response to the control signal when packaged into a second

package form," as claimed in amended independent claim 1, or "each of the plurality of generic pads" that are used as a "data IO pad in response to a control signal when packaged into a first package form" and that are used as an "address pad in response to the control signal when packaged into a second package form," as claimed in amended independent claim 9.

Since the combination of AAPA and Choi fails to teach or suggest the invention set forth in the amended claims, the claims are believed to be allowable over the cited references. Accordingly, reconsideration and removal of the rejection of claims 1, 3, 4, 9, 11, and 12 under 35 U.S.C. 103(a) based on the combination of AAPA and Choi are respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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